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Priority Cache Object Replacement by Using LRU, LFU, and FIFO Algorithms to Improve Cache Memory Hit Ratio

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Abstract

Due to the increasing CPU and cache memory performance, using replacement algorithms is very important in various aspects of high-performance computing environments such as e-commerce systems, cache memory management in microprocessors, object management in operating systems, iteration strategies in information distribution systems, etc. Database server cache performance is an essential issue in e-commerce systems. Managing the entry and exit of cache objects with replacement algorithms can reduce the workload of the database server and improve server performance. The algorithms determine which objects remain in the cache memory and which go out to make room for new objects. In this way, the algorithms decrease user access time and enhance the system's performance. Most of these algorithms are developed by the famous LRU and LFU schemes and can fix their flaws; however, unlike them, they are challenging to implement. This research proposes a priority object replacement algorithm that is easy to implement. The PCORA algorithm is based on prioritizing cache memory objects according to three parameters. Experiments show that the proposed algorithm has a better hit ratio than others and can improve cache memory performance.

Keywords: Operating systems, Cache memory management, E-commerce systems, Replacement algorithms, Hit ratio, Performance.

1 | Introduction

The rapid rise of the world wide web has led to an increase in the visibility of web traffic and delays in its access. One of the areas affected by this problem is database servers in systems with e-commerce applications. Database server cache performance is an important issue in e-commerce systems [1]. Managing the entry and exit of cache objects can reduce the workload of the database server and improve server performance. Web caching is one of the most effective techniques proposed to solve this problem [2]. Two methods have been

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proposed to enhance the performance of the cache memory effectively: One is to increase the size of the cache memory, which is very expensive. The second method is to design a useful cache memory replacement algorithm. Caching is a popular performance optimization method that is widely used in web storage. If there is not enough cache memory, the load on the servers will increase as the number of users and their requests increases. This can cause network traffic problems and network delays [3]. There are three patterns of web cache memory for cache memory: Client-side cache memory, server-side cache memory, and proxy cache memory [4]. Client-side cache memory refers to cache memories on the user side that store web page addresses and other information to use that information to access servers. Server-side cache memory refers to creating a cache memory on the web server side. It aims to reduce the number of server requests, which can reduce server load. Proxy cache memory usually interfaces between the user's and central servers. When a user sends a request to a central server via a proxy server, the server sends the data to the user according to the main request path. During this procedure, the proxy server decides whether or not to save a copy in its cache memory, as this data may be requested in the future. Therefore, using an alternative algorithm for server-side cache memory and proxy server to reduce network delay is more important. Many factors affect the efficiency of cache memory, the most important of which are the frequency of access, the last access time, and the size of the cache memory object.

For each factor, researchers have proposed appropriate algorithms. When the cache is full, they all have their algorithm to choose which object to delete. The cache memory replacement policies generally aim to enhance the cache memory hit rate. Hit rate is a standard for measuring the performance of web cache memory replacement algorithms. The higher the hit rate, the better the replacement algorithm [5]. This research proposes a cache memory replacement policy with a high hit rate and low delay, which is easy to implement, to improve cache memory performance. This algorithm, named Priority Cache Object Replacement Algorithm (PCORA), is based on prioritizing cache memory objects according to three parameters [6]. PCORA, which has a priority model, takes advantage of existing cache memory replacement algorithms, which makes the proposed algorithm more accurate and reliable.

The rest of the paper is organized as follows: In Section 2, a review of the past literature is done, and the strengths and weaknesses of each are described. Section 3 separately describes each part of the PCORA algorithm, including the data and its main and sub-functions. In Section 4, the performance of the proposed algorithm is evaluated in terms of hit ratio and compared with other algorithms. Section 5 concludes the proposed algorithm and suggests future research works.

2 | Literature Review

In this section, famous algorithms affecting systems and other existing algorithms are reviewed, and their advantages and disadvantages are stated.

When the cache memory is full and a new object needs to be stored, a replacement algorithm should select which object must be deleted to make room for the new object [7]. Cache memory replacement algorithms select which data can stay in the cache memory. An effective cache memory replacement algorithm has less error and can improve cache memory hit and byte rates [8]. Many academic and industry researchers are trying to find an optimal cache memory replacement policy. According to *Table 1*, conventional cache memory replacement algorithms are mainly divided into 5 categories [5], [9].

Table 1. Five conventional cache memory replacement algorithms.

Algorithm	Brief Description	Advantages	Disadvantages
RAND	A random number generator to identify an alternative object	It is the simplest algorithm and easy to implement.	It is not considered as any factor. It has an unstable performance. Its hit rate is low.

Table 1. Cotinued.

Algorithm	Brief Description	Advantages	Disadvantages
LAURA	The least used items are deleted first.	It is easy to implement and has a low hit rate.	No factor other than the time factor is considered It contains the cache contamination.
LFU	Objects of the least frequency are removed first.	It prevents cache memory contamination.	Only the frequency factor is considered, and other factors are ignored. It isn't easy to implement.
SIZE	Large objects are removed first.	It is easy to implement, preserves small objects first, and has a high cache hit rate.	It first stores small web objects even if they are not re-accessed. It has a low byte hit rate.
GDSF	Frequency and launch factors are combined, and the age factor is produced like the time factor.	It covers the weakness of the sizing algorithm by deleting objects that are no longer accessible to users.	Its computational cost is low, and it has a complex parameter setting. It has a low byte hit rate.

In the recent LRU algorithm, time is the main factor. The basic idea of this algorithm is that if data is recently requested, it will be more likely to be requested in the future. When the cache memory is full, it deletes less recently mentioned objects. The advantage of this model is that it has good performance and is very easy to implement on the client side. However, this algorithm only considers the last visit and does not care about the number of visits to an object [3], [5]. In the LFU algorithm, researchers consider popularity or the number of visits to the object as the main factor. The basic idea is that the more data you refer to, the more likely you will refer to them. It is commonly used to store web URLs, and when the cache memory is full, it removes the web object with the least number of visits.

The advantage is that it is also easy to implement and works well on the proxy side [10], [11]. In a weight-based algorithm, researchers use weights to decide which object should be cleared from the cache memory. Weight is classified in descending order. Users can directly remove the object with the biggest weight [12]. FPRA is a modification of popular alternative algorithms such as LRU and LFU. This algorithm uses FCM to cluster pages based on three parameters. Clusters of higher freshness, higher frequency, and lower referral rates have higher priority [13]. Clustering allows pages that are more similar to each other to be in the same group [14].

Arya et al. [15] have developed a new concept for page replacement based on reading page blocks from secondary memory. Whenever there is an error on the page, instead of reading only one missing page, the property of the pages equal to the number of frames allocated to that process is restored. This way, the number of page errors is minimized, increasing the hit rate. In [16], a cache memory replacement policy based on the FHPA algorithm is proposed, which restricts the full use of device space with an edge. Considering the heat of the file, the possibility of re-accessing the file cache is evaluated. The cached file with the least chance of being re-accessed will be removed from the cache memory.

In [17], a new cache memory replacement policy is proposed to enhance embedded processors' last-level cache memory effectiveness. Unlike LRU, this algorithm uses the correlation of the distance among the tags between the cache memory lines to improve accuracy. Shin et al. [18] presented a new cache memory management scheme for rendering systems. Unlike public-purpose computing systems, rendering systems display specific file access patterns that significantly disrupt the performance of the buffer cache memory system. Different input and output sequences of rendered files are collected to deal with this situation, and their access patterns are analyzed. The WRP algorithm has two major problems. The first problem of this algorithm occurs when the result of dividing two factors (novelty and frequency) for one block is equal to another. The second problem is that it only considers the time interval between the last two accesses and does not consider the previous accesses.

In [19], these two problems and other small problems are solved by introducing a new function. Anwar et al. [20] proposed a buffer storage replacement algorithm for flash-based storage devices. Being called the LBA, it considers that flash memory has asymmetric reading and writing costs. In [21], the impact of the cost of the last-level cache memory in a hybrid memory system was mainly addressed. A cost cache memory replacement policy in shared-level cache memory has been proposed to increase memory performance. CACRP improves cache memory performance by three parameters.

The WOLF-ARE algorithm counters network traffic and recognizes popular files. This algorithm considers the frequency and recent information of the files to determine the popularity of the content [22]. The CCF-LRU policy categorizes data sheets with cold or hot attributes and clean or dirty properties. The replacement algorithm concept is to replace as many cold and clean data sheets as possible, especially those that have been referenced only once before switching hot pages [23], [24].

Jiang and Zhang [25] proposed a cache memory algorithm for HetNets with SBSs, MBS, and D2D transfers. They mixed cache strategy design as an integer linear programming problem to minimize system costs. The RCR algorithm considers the temporary location of traffic. If a cache memory error occurs and the current traffic location is close to the missing rule, a victim rule is replaced with the miss cache rule, and a high value is set for the missing rule to keep the rule in TCAM [26]. The basic idea of the CLOCK-DNV algorithm is to share all the free space in NVM and DRAM and manage the DRAM space in a page granulation and the NVM space in a block granulation to use temporal and spatial locality [27]. PLRU and PLFU algorithms keep 20% of the top popular movies of each video group in Memcached without choosing them as alternative candidates [28].

Karami and Guerrero-Zapata [29] proposed an ANFIS-based cache memory replacement algorithm to reduce two general cache infection attacks: Incorrect location and location disruption in NDN. This algorithm is very effective in determining and reducing fake content. The AC-CLOCK screen replacement algorithm takes advantage of both DRAM and PCM algorithms. DRAM has unlimited writing, shorter writing delays, higher density, and less static power [30]. WGDSF is based on a weight substitution algorithm that uses a new weight and cost strategy. In addition, it takes advantage of the existing cache memory replacement policy. WGDSF is a developed GDSF algorithm, and its implementation is based on the type of weight document and time-based on weight frequency.

The weight frequency-based time parameter is a keyword that indicates the content's popularity and has a large number in the cache memory replacement process [31]. LER focuses on the above writing error in STT-RAM cache memories from transactions 0 to 1. The basic idea is to place the input object in a cache memory line with the least error in the writing operation [32]. Motwani et al. [33] developed a new algorithm that enhances the performance of multi-level cache memory. In the proposed algorithm, an object's reference value depends on the object's freshness in the cache memory, along with the novelty characteristics and frequency of the object. Nomura [34] proposed delaying the decision to freeze cache memory line layouts to implement the Stubborn strategy more effectively.

Olanrewaju et al. [35] proposed the NB-AWRPDA smart web proxy memory approach aiming to improve AWRP performance in terms of HR and BHR. By studying the various page replacement algorithms, it should be noted that the LRU algorithm has better results than many other policies and it is possible to improve it [36]. The HCR algorithm selects and sacrifices a block with the least probability of error and the minimum number of writes during the write operation from a set of blocks [37]. ICRA is a cache memory replacement policy combined with an indexing policy, and its main innovation is that when the document and page information are read for the first time, an index is created. The indexed data is analyzed, sorted, and stored in the cache memory [38].

PR-LRU increases flash memory performance and reduces writing count. This algorithm divides the buffer into the victim, cold, hot, and LRUs. Pages from the cold or hot LRU list are placed in the victim LRU list. The victim LRU list prefers to replace clean pages with dirty ones [39]. Chen et al. [40] proposed a lightweight chart transformation method that provides a custom cache for full use of chart-level data reuse. They also propose a mapping method that uses data parallelization and reuse to manage different graphs' input effectively. The proposed method increases the memory cache efficiency of database servers for e-commerce applications by reducing server overload. In [41], the subject of identifying fake ideas in e-commerce businesses based on short-term memory is a repetitive deep-learning neural network. The test was performed using the standard Yelp product review dataset. A linguistic query and word count dictionary were used to extract additional linguistic features from the review texts, which can help distinguish between real and fake comments.

He and lin [42], proposed horizontal position design method in a single-user buffer auxiliary relay system and a 3D position design method in a multi-user buffer auxiliary relay system. The positioning system is designed to be achieved with the maximum system average and optimal speed. The proposed method significantly improves performance in the convergence of power, speed, path losses, and energy costs, which can provide higher-quality communication services to users in the system and better support for the widespread use of drones.

In general, among the algorithms proposed to solve the problem of speed difference between CPU and cache, the optimal algorithm has good performance and is easy to implement. This research proposes a priority object replacement algorithm called PCORA, which is based on prioritizing cache memory objects according to three parameters. Experiments show that the proposed algorithm has a better hit rate than other algorithms and can effectively improve cache memory performance.

3 | Priority Cache Object Replacement Algorithm

This section separately describes each part of the Priority Cache Object Replacement Algorithm (PCORA) algorithm, including the data and its main and sub-functions.

PCORA is based on prioritizing cache memory objects and takes advantage of existing cache memory replacement algorithms, which makes it more reliable and more accurate [43]. This method offers an approach that improves the hit rate of the cache memory and uses as much cache space as possible. Three cases happen when users request an object on the network. In the first case, if the requested object is in the cache memory, a hit occurs, and the request is answered. In the second case, if the requested object is not in the cache memory and the cache memory capacity is sufficient, an error occurs and that object will be added to the cache memory. In the third case, if the requested object is not in the cache memory and the cache capacity is insufficient, an error occurs, and one of the cache memory objects must be removed to save the new object. In this case, PCORA uses the priority function to decide which object should be removed from the cache memory.

The proposed replacement algorithm is a powerful tool that can increase server performance by considering three factors: Recency, frequency, and input order of each object. It runs similarly to the LRU and LFU algorithms and prioritizes each object according to both factors. The first factor, RecP (j), is a counter that indicates the freshness of object j in cache memory and the second factor, FreP (j), is a counter that shows the number of times object j is requested in cache memory. Based on the two factors RecP (j) and FreP (j), the value of the object j priority function is calculated by *Model (1)*.

$$\mathrm{Per\,P_j} = \frac{\mathrm{Re\,c\,P_j}}{\mathrm{Fre\,P_j}}. \tag{1}$$

An object in the cache memory whose priority function value is higher than the others has the highest priority for deletion from the cache memory. The third factor, IOP(j), is the order in which object j enters the cache memory. When the new object j is placed in the cache memory, the priority function factors must be initially quantified. According to the above variables, PCORA is run based on the following five functions:

3.1|The Main Function

In the main function, when object j is requested, one of the proposed algorithm's three main function modes occurs.

```
Main Function
For each requested object, j
    If (the requested object j is not in the cache and the cache
       is not full)
         call Function 1
       else if (the requested object j is in the cache)
         call Function 2
       else if (the requested object j is not in the cache and the
          the cache is full)
       call Function 3
```

3.1.1|Function 1

When the cache memory is referred to, the requested object j is not available, and the cache memory is not full, a Miss occurs, and the requested object must be added to the cache memory. In such cases, *Function 1* is executed.

```
Function 1
For each frame in the cache memory
    If (the frame i is empty) then
       Place the new object in frame i in the cache memory
       RecP(j)=1
       FreP(j)=1
       IOP(j) = Cache Size
```

Set the RecP (j) factor to 1, FreP (j) to 1, and IOP (j) to the number of cache memory frames. FreP (j) is set to 1 because this means that object j is used once, and IOP (j) is equal to the size of the cache memory because object j is stored as the last object in the cache memory, and it should be at the end of the queue like the FIFO algorithm.

3.1.2|Function 2

At each access to the cache memory, if the requested object j exists in the cache memory, a hit occurs, and *Function 2* is executed.

```
Function 2
If requested object j is in the cache
  For each object i in the cache
    If  $i \neq j$
          RecP(i) = RecP(i) +1
       RecP(j) =1 and  FreP(j) = FreP(j) +1
```

3.1.3|Function 3

When the cache memory is accessed, the requested object j is not in the cache memory, and the cache memory is full; in this case, the proposed algorithm updates the PreP value and selects the object with the maximum value of the priority function. If there is more than one object with the maximum value of the priority function, among the objects with the maximum value, an object with the minimum IOP value is selected to be deleted from the cache memory. The object with the maximum value of the priority function is searched top-down in the cache memory. Suppose an error occurs; the algorithm must select object t with the maximum value of the priority function and clear it from the cache memory; in such a case, *Function 3* will be executed.

```
Function 3
Update the PreP
    If there is only one maximum PreP
      Remove the object with maximum PreP (object t)
    else
      Remove the object with maximum PreP and
      minimum IOP
    For each object(i) in the cache
      If   $i \neq j$ and $i \neq t$

        $RecP(i) = RecP(i) + 1$,
        $RecP(t) = RecP(t) + 1$  and  $FreP(t) = 1$,
        $RecP(j) = 1$ and  $FreP(j) = FreP(j) + 1$ and  $IOP(j) =$ Cache Size.
    For each object(i) in the cache,
      If   $IOP(i) > IOP(t)$,

          $IOP(i) = IOP(i) - 1$.
```

One of the important concepts in replacement algorithms is their high overhead on systems. The proposed algorithm requires three counters to run, which adds memory overhead to the system: First, the algorithm requires a counter for RecP (j); second, a counter for FreP (j); and third, a counter for IOP (j). The last and maximum space required is the space for PreP (j), which is the value of the priority function of each object in the cache memory. Calculating the value of the priority function of each object reduces memory time and overhead only if the requested object j is not in the cache memory and the cache memory is full. The proposed algorithm for solving this problem considers PreP (j) as an integer to reduce the main costs.

4 | Performance Evaluation

In this section, the performance of the proposed algorithm is evaluated experimentally.

The proposed algorithm was simulated with C# programming language and compared to six algorithms: LRU [3], [5], FIFO [36], WRP [12], LFU [11], [16], MFU [9], and DWRP [19]. The emulator is designed to execute some address sequences, provide instructions for some real applications, and implement various replacement algorithms with different cache memory sizes. The hit rate obtained depends on the locality of the cache memory access requests, the cache memory size, and the replacement algorithm. The modular design of the emulator allows easy simulation and optimization of the proposed algorithm. An address sequence is a list of thousands of memory addresses generated by a real program running on a processor. The addresses come from executing storage and code retrieval instructions. Some address sequences include instructions for both data and fetch addresses, but only one data cache memory is simulated; therefore, the sequences have only data addresses.

Three sequences derived from SPEC standards have been used to simulate the proposed algorithm. According to the sequences used, four cache memory sizes are considered and the emulator is run to evaluate the performance of the proposed algorithm. The emulator runs with 4 different cache memory sizes for the NNgcc address sequence, and the results are compared to LRU, FIFO, WRP, LFU, MFU, and DWRP algorithms. *Table 2* shows the hit rate values for the NNgcc address sequence simulated by LRU, FIFO, WRP, LFU, MFU, DWRP, and PCORA. When the cache memory size is 1K, the performance of the proposed algorithm is 64.046% better than DWRP. Moreover, when the cache memory size is 0.5K, the PCORA hit rate is 2.322% higher than the best algorithm, the LRU. In the worst case, when the cache memory size is 3K, it works 0.402% better than the LRU.

As shown in *Fig. 1*, PCORA performs significantly better than the other six algorithms. The hit rate obtained from PCORA with NNsixpack address sequence is above 60.24%; this rate is between 52.4% and 58.958% for LRU and between 9.234% and 26.656% for DWRP (*Table 3*). As shown, as the cache memory size increases, the performance of the proposed algorithm increases. *Fig. 2* shows the PCORA simulation results compared to the other 6 algorithms in which it performs better than the others. The third address sequence is NNswim. *Fig. 3* shows the comparison and the result of this sequence. *Table 4* shows the exact hit rates of seven algorithms with cache memory sizes of 0.5K, 1K, 2K, and 3K. The results show that the maximum hit rate is related to the LRU algorithm with the largest cache memory size, which is about 84.082%. The result for the proposed algorithm is expected to be at least equal to the highest value among the other six algorithms or more. The results in *Table 4* showed that the maximum hit ratio for PCORA is about 84.692%. This is 0.61% higher than the best hit rate for the LRU and 18.59% higher than the worst hit rate for the MFU. As explained, in all the sequences used, the hit rate of the proposed algorithm is always better than that of other alternative algorithms. This is due to the priority factors considered in PCORA that never allow the result to be worse than the maximum hit rate of the other 6 alternative algorithms.

Table 2. A comparison between hit ratio of different algorithms with 4 cache sizes (NNgcc).

Cache Size	PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
512 (0.5k)	65.864	63.542	61.684	59.042	34.642	46.952	11.93
1024 (1k)	76.256	75.754	72.51	66.584	47.836	48.684	12.21
2048 (2k)	80.618	79.784	77.668	74.442	64.268	50.758	33.948
3072 (3k)	82.244	81.842	80.95	76.874	81.256	51.656	60.19

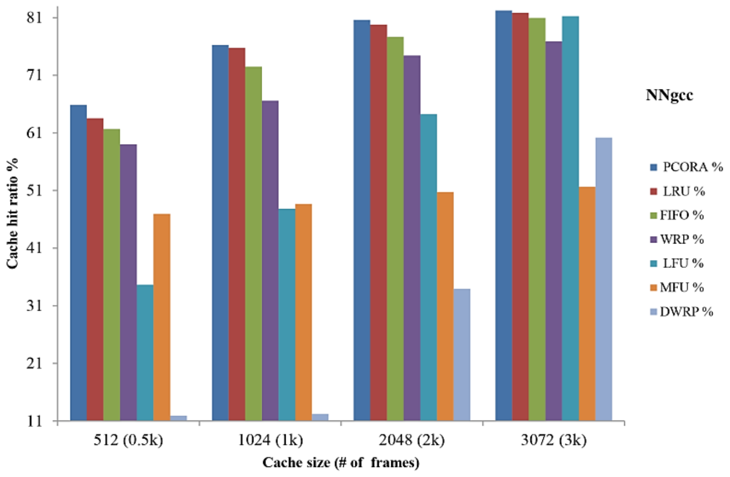

Fig. 1. Performance of different algorithms with different cache sizes for NNgcc.

Table 3. A comparison between hit ratio of different algorithms with 4 cache sizes (NNsixpack).

Cache Size	PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
512 (0.5k)	53.016	52.4	51.37	49.264	24.244	37.822	9.234
1024 (1k)	55.466	54.92	54.206	53.686	33.564	38.98	9.552
2048 (2k)	58.332	57.8	57.032	57.49	42.446	40.342	13.378
3072 (3k)	60.24	58.958	58.4	59.458	55.808	41.124	26.656

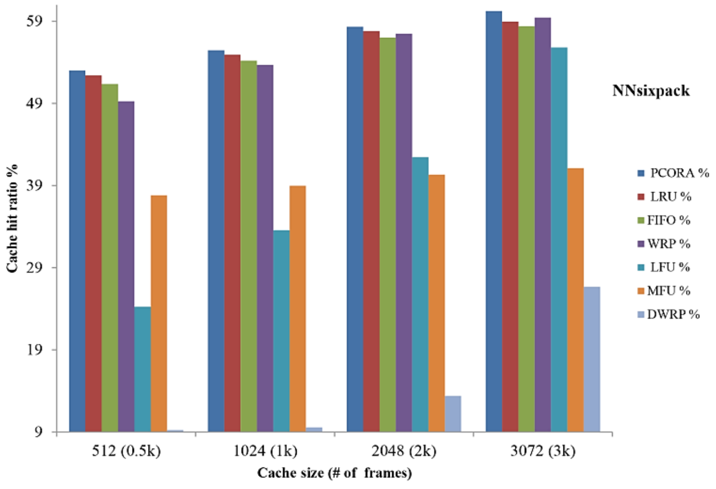

Fig. 2. Performance of different algorithms with different cache sizes for NNsixpack.

Table 4. A comparison between hit ratio of different algorithms with 4 cache sizes (NNswim).

Cache Size	PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
512 (0.5k)	79.696	79.104	76.95	70.294	66.29	50.066	23.12
1024 (1k)	80.974	80.52	79.098	74.34	72.822	53.868	33.036
2048 (2k)	83.438	82.572	81.464	77.052	78.756	59.038	56.296
3072 (3k)	84.692	84.082	83.24	79.638	83.128	66.102	78.652

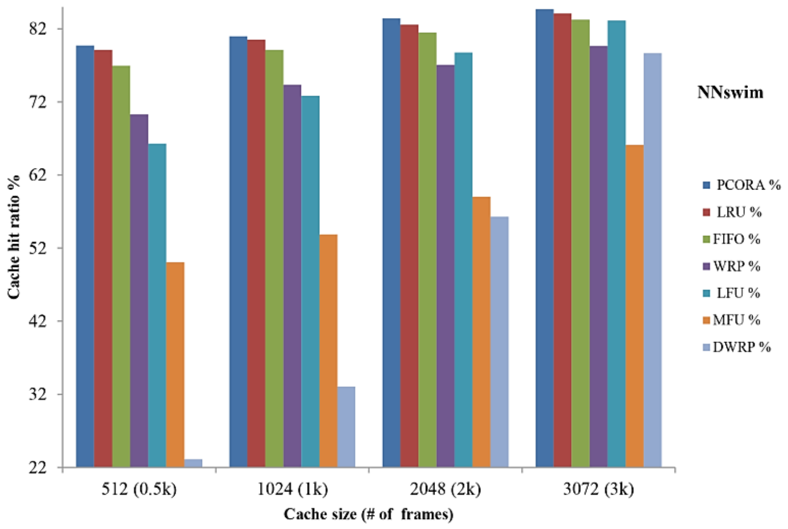

Fig. 3. Performance of different algorithms with different cache sizes for NNswim.

The emulator also calculates the average hit rates of PCORA, LRU, FIFO, WRP, LFU, MFU, and DWRP algorithms with three address sequences. The results are presented in *Tables 5-7*. *Fig. 4* shows that when the NNgcc address sequence is used, the average PCORA performance 4 is better than other algorithms. *Table 5* shows the average 4 hit rates of seven algorithms for the NNgcc address sequence. The performance of the proposed algorithm is 1.015% better than the best algorithm, LRU, and 46.676% better than the worst algorithm, DWRP. As shown in *Fig. 5* and *Fig. 6*, PCORA performs better than other algorithms, details of which are given in *Table 6* and *Table 7* for the NNsixpack and NNswim address sequences, respectively.

Table 5. A comparison between average 4 hit ratios of different algorithms (NNgcc).

PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
76.2455	75.2305	73.203	69.2355	57.0005	49.5125	29.5695

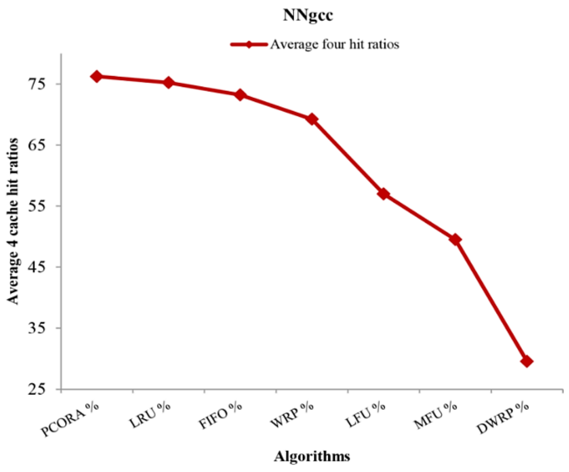

Fig. 4. Average four performances of different algorithms for NNgcc.

Table 6. A comparison between the average four hit ratios of different algorithms (NNsixpack).

PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
56.7635	56.0195	55.252	54.9745	39.0155	39.567	14.705

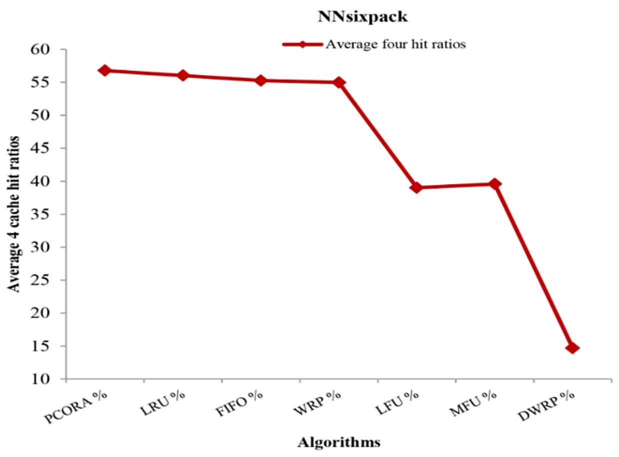

Fig. 5. Average 4 performances of different algorithms for NNsixpack.

Table 7. A comparison between average 4 hit ratios of different algorithms (NNswim).

PCORA%	LRU%	FIFO%	WRP%	LFU%	MFU%	DWRP%
82.2	81.5695	80.188	75.331	75.249	57.2685	47.776

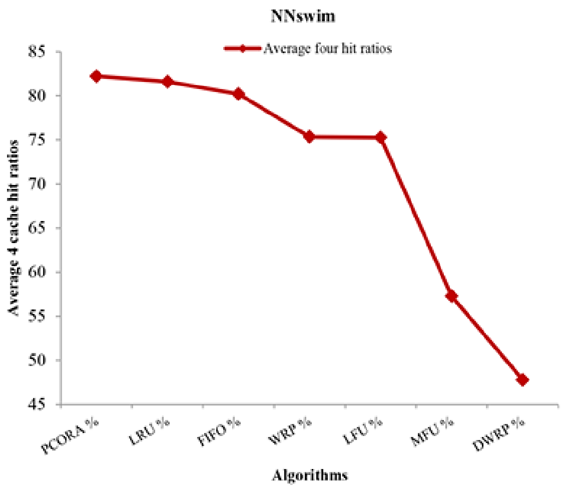

Fig. 6. Average four performances of different algorithms for NNswim.

5 | Conclusion

In this research, a cache memory replacement algorithm was introduced. A simulation of cache memory with a sequence of different addresses showed that it was a modification for popular replacement algorithms such as LRU and LFU. It indicated that objects with a smaller priority function value are more likely to be re-requested than others. PCORA was simulated with three address sequences and compared to six popular algorithms. The PCORA simulation result with four different cache memory sizes performed better than the other six algorithms. The algorithm can be simulated with other address sequences and algorithms. It should be noted that other parameters and factors that indicate the properties of objects in the cache memory can be considered for the proposed algorithm. For example, considering the size and cost of each object in the cache memory makes PCORA perform better for applications such as web storage. The proposed design is also suitable for deciding on centralized cache memory but not for a distributed solution.

Conflict of Interest

The authors declare no conflict of interest.

Ethical Approval

This article contains no studies with human participants or animals performed by authors.

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